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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,554	03/25/2004	Gary Dean Anderson	AUS920030980US1	7924

35525 7590 03/06/2007

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,554	ANDERSON ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- **Claims 1-2, and 4-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ademmer, et al, U.S. Patent Number 6,212,643.**

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, and 4-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ademmer, et al, U.S. Patent Number 6,212,643.

3. Regarding claim 1:

a. Regarding the limitation of "identifying, by a service processor, failed hardware of the computer system," Ademmer discloses a system with a, and a link between them. (Lines 1-6 of Column 2). Ademmer discloses that the system controller can identify a failure. (Lines 13-15 of Column 1).

b. Regarding the limitation of "identifying, by a service processor, other hardware affected by the failed hardware within the computer system," Ademmer discloses a system wherein the device controller can identify hardware as having a failure via a POST test. (Lines 37-39 of Column 2).

c. Regarding the limitation of "deconfiguring the failed hardware and the other hardware affected by the failed hardware," Ademmer discloses a system that can deactivate a hardware component and save the information of configuration on CMOS-ROM. (Lines 45-55 of Column 2).

d. Regarding the limitation of "rebooting the computer system without running a diagnostic on the failed hardware," Ademmer discloses a system that can deactivate a hardware component and upon reactivation, does not test or diagnose the hardware. (Lines 55-57 of Column 2).

4. Regarding claim 2, Ademmer disclose that a device controller disconnect the system and reconnects it upon activity being detected. (Lines 1-11 of Column 3).

5. Regarding claim 4, Ademmer discloses a system with a, and a link between them with a switch to turn the hardware device on and off. (Lines 1-6 of Column 2).

6. Regarding claim 5, Ademmer discloses a system wherein a CMOS-RAM stores information regarding the state of the hardware device. (Lines 45-57 of Column 2).

7. Regarding claim 6:

e. Regarding the limitation of "identifying, by a service processor, failed hardware of the computer system," Ademmer discloses a system with a, and a link between them. (Lines 1-6 of Column 2). Ademmer discloses that the system controller can identify a failure. (Lines 13-15 of Column 1).

f. Regarding the limitation of "identifying, by a service processor, other hardware affected by the failed hardware within the computer system," Ademmer discloses a system wherein the device controller can identify hardware as having a failure via a POST test. (Lines 37-39 of Column 2).

g. Regarding the limitation of "deconfiguring the failed hardware and the other hardware affected by the failed hardware," Ademmer discloses a system that can deactivate a hardware component and save the information of configuration on CMOS-ROM. (Lines 45-55 of Column 2).

h. Regarding the limitation of "rebooting the computer system without running a diagnostic on the failed hardware," Ademmer discloses a system that can deactivate a hardware component and upon reactivation, does not test or diagnose the hardware. (Lines 55-57 of Column 2).

8. Regarding claim 7, Ademmer discloses a system with a, and a link between them with a switch to turn the hardware device on and off. (Lines 1-6 of Column 2).

9. Regarding claim 8, Ademmer discloses a system wherein a CMOS-RAM stores information regarding the state of the hardware device. (Lines 45-57 of Column 2).

10. Regarding claim 9, Ademmer disclose that a device controller disconnect the system and reconnects it upon activity being detected. (Lines 1-11 of Column 3).

11. Regarding claim 10:

i. Regarding the limitation of "identifying, by a service processor, failed hardware of the computer system," Ademmer discloses a system with a, and a link between them. (Lines 1-6 of Column 2). Ademmer discloses that the system controller can identify a failure. (Lines 13-15 of Column 1).

j. Regarding the limitation of "identifying, by a service processor, other hardware affected by the failed hardware within the computer system," Ademmer discloses a system wherein the device controller can identify hardware as having a failure via a POST test. (Lines 37-39 of Column 2).

k. Regarding the limitation of "deconfiguring the failed hardware and the other hardware affected by the failed hardware," Ademmer discloses a system that can deactivate a hardware component and save the information of configuration on CMOS-ROM. (Lines 45-55 of Column 2).

l. Regarding the limitation of "rebooting the computer system without running a diagnostic on the failed hardware," Ademmer discloses a system that can deactivate a hardware component and upon reactivation, does not test or diagnose the hardware. (Lines 55-57 of Column 2).

12. Regarding claim 11, Ademmer discloses a system with a, and a link between them with a switch to turn the hardware device on and off. (Lines 1-6 of Column 2).

13. Regarding claim 12, Ademmer discloses a system wherein a CMOS-RAM stores information regarding the state of the hardware device. (Lines 45-57 of Column 2).

14. Regarding claim 13, Ademmer disclose that a device controller disconnect the system and reconnects it upon activity being detected. (Lines 1-11 of Column 3).

15. Regarding claim 14, Ademmer discloses a system wherein a CMOS-RAM stores information regarding the state of the hardware device. (Lines 45-57 of Column 2).

16. Regarding claim 15, Ademmer discloses a system wherein a POST test can occur to test interactions of a plurality of components. (Lines 30-53 of Column 2).

17. Regarding claim 16, Ademmer discloses a system wherein the system can resume operations if no error exists. (Lines 1-11 of Column 3).

18. Regarding claim 17, Ademmer discloses a system wherein a POST test can occur to test interactions of a plurality of components. (Lines 30-53 of Column 2).

19. Regarding claim 18, Ademmer discloses a system wherein the system can resume operations if no error exists. (Lines 1-11 of Column 3).

20. Regarding claim 19, Ademmer discloses a system wherein a POST test can occur to test interactions of a plurality of components. (Lines 30-53 of Column 2).

21. Regarding claim 20, Ademmer discloses a system wherein the system can resume operations if no error exists. (Lines 1-11 of Column 3).

Response to Arguments

22. Applicant's arguments with respect to claim 1-2, 4-20 have been considered but are moot in view of the new ground(s) of rejection.

23. Applicant's arguments, filed 12/14/2006, with respect to the objection to claim 3 have been fully considered and are persuasive. The objection of claim 3 has been withdrawn due to the cancellation of the claim.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

27. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

28. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

30. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

31. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

tmb
March 2, 2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER